

FIG. 1

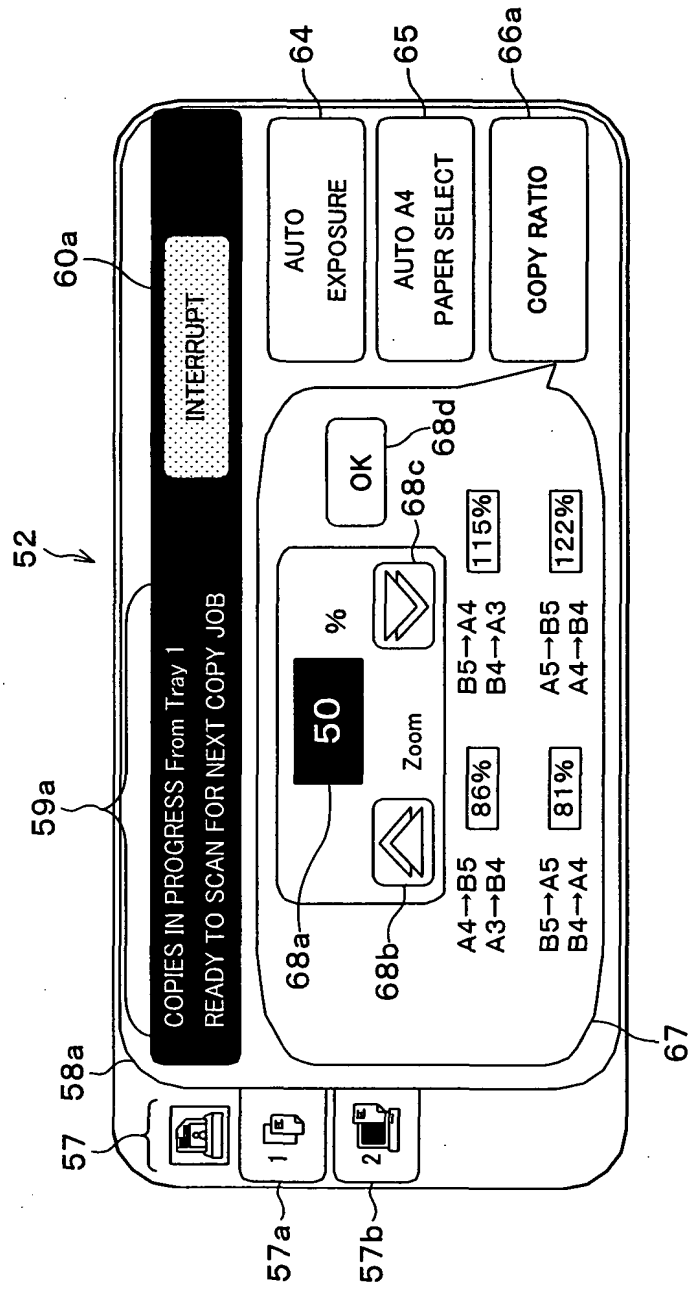
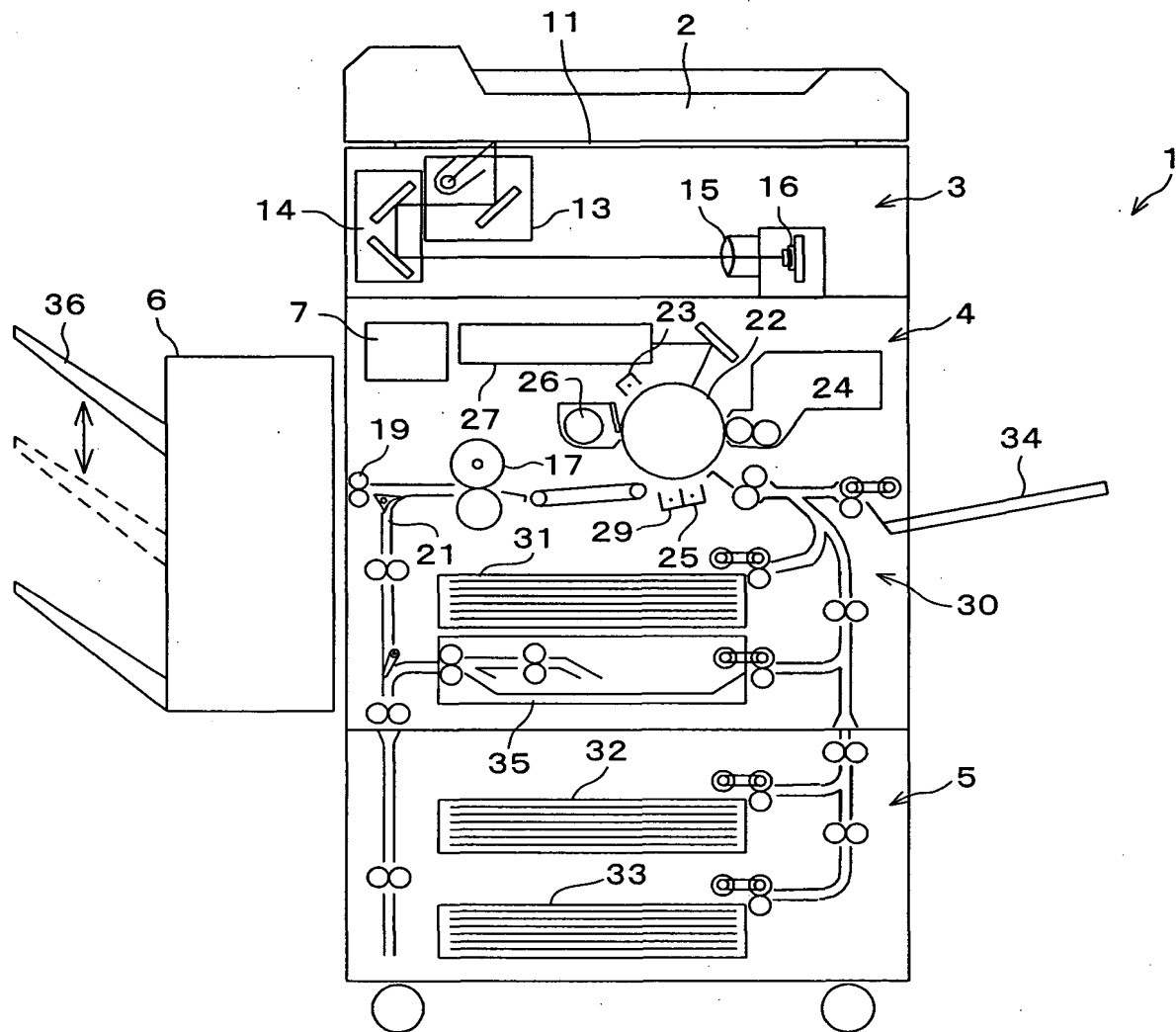


FIG. 2



The block diagram illustrates the system architecture, centered around a **CENTRAL PROCESSING SECTION (7a)**. The system components and their interconnections are as follows:

- OPERATION PANEL (50)**: Contains a **HARD KEY GROUP (51)**, an **LCD (52)**, and a **DISPLAY CONTROL SECTION (69)**.
- POST PROCESS CONTROL SECTION (48)**: Connected to the **CENTRAL PROCESSING SECTION (7a)** and the **CONVEYING SYSTEM DRIVE SECTION (49)**.
- CONVEYING SYSTEM DRIVE SECTION (49)**: Connected to the **POST PROCESS CONTROL SECTION (48)**.
- AUTOMATIC DOCUMENT FEEDER DRIVE SECTION (44)**: Connected to the **CENTRAL PROCESSING SECTION (7a)** and the **DISPLAY CONTROL SECTION (69)**.
- FEEDER'S SHEET CONVEYING SYSTEM DRIVE SECTION (46)**: Connected to the **CENTRAL PROCESSING SECTION (7a)**.
- DOCUMENT READING DRIVE SECTION (45)**: Connected to the **CENTRAL PROCESSING SECTION (7a)**.
- IMAGE FORMATION DRIVE SECTION (47)**: Connected to the **CENTRAL PROCESSING SECTION (7a)**.
- IMAGE DATA INPUT SECTION (40)**: Receives data from the **CCD (16)** and sends it to the **IMAGE PROCESSING SECTION (7b)**.
- IMAGE PROCESSING SECTION (7b)**: Connected to the **CENTRAL PROCESSING SECTION (7a)**, **MAIN MEMORY (7c)**, and **IMAGE DATA OUTPUT SECTION (42)**.
- IMAGE DATA OUTPUT SECTION (42)**: Receives data from the **IMAGE PROCESSING SECTION (7b)**.
- MAIN MEMORY (7c)**: Connected to the **IMAGE PROCESSING SECTION (7b)** and the **HARD DISC (41)**.
- IMAGE DATA COMMUNICATION I/F (43)**: Connected to the **MAIN MEMORY (7c)**.
- HARD DISC (41)**: Connected to the **MAIN MEMORY (7c)**.

The **CENTRAL PROCESSING SECTION (7a)** is the core of the system, managing the flow of data and control signals between the various drive sections, input/output sections, and memory components.

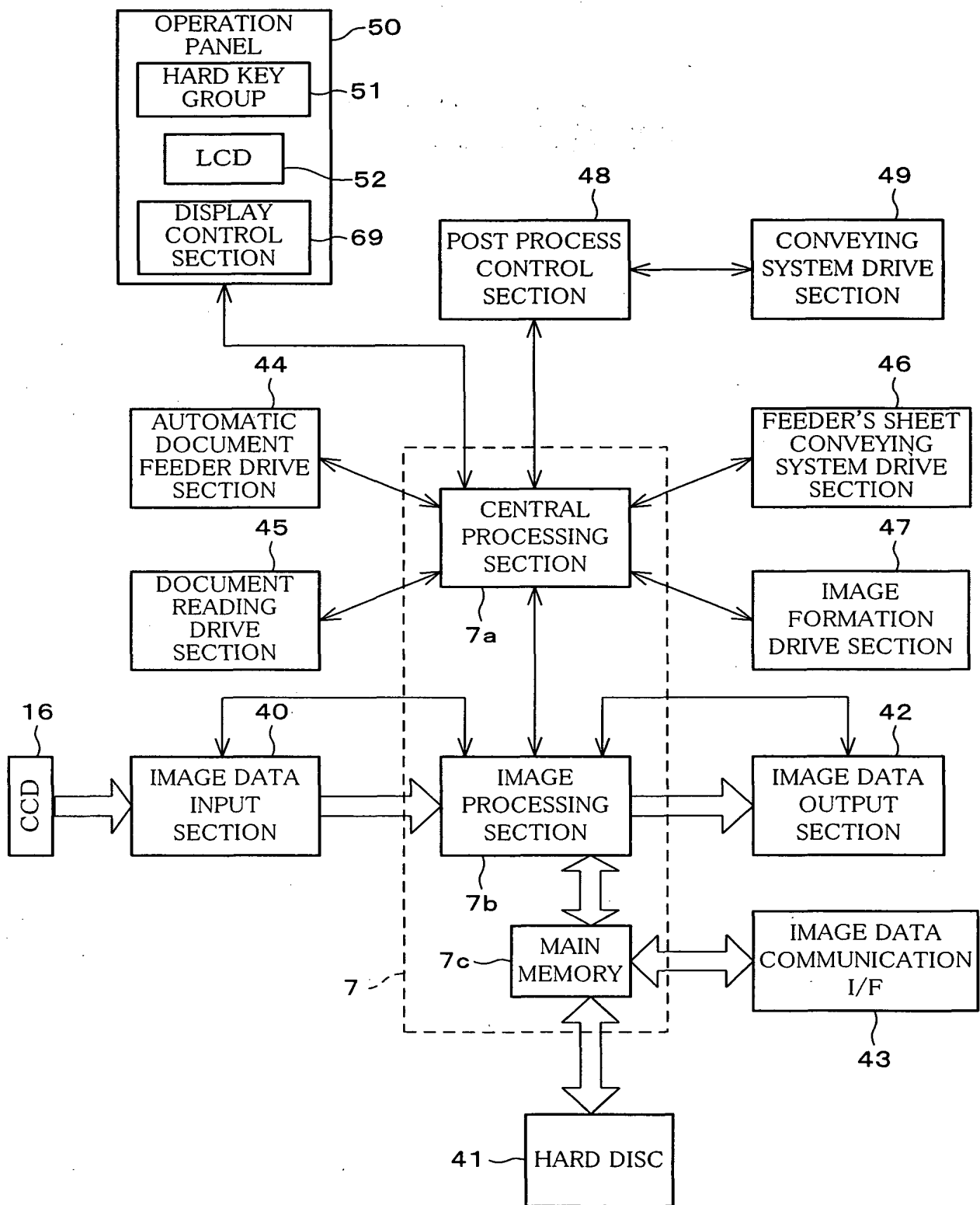


FIG. 4

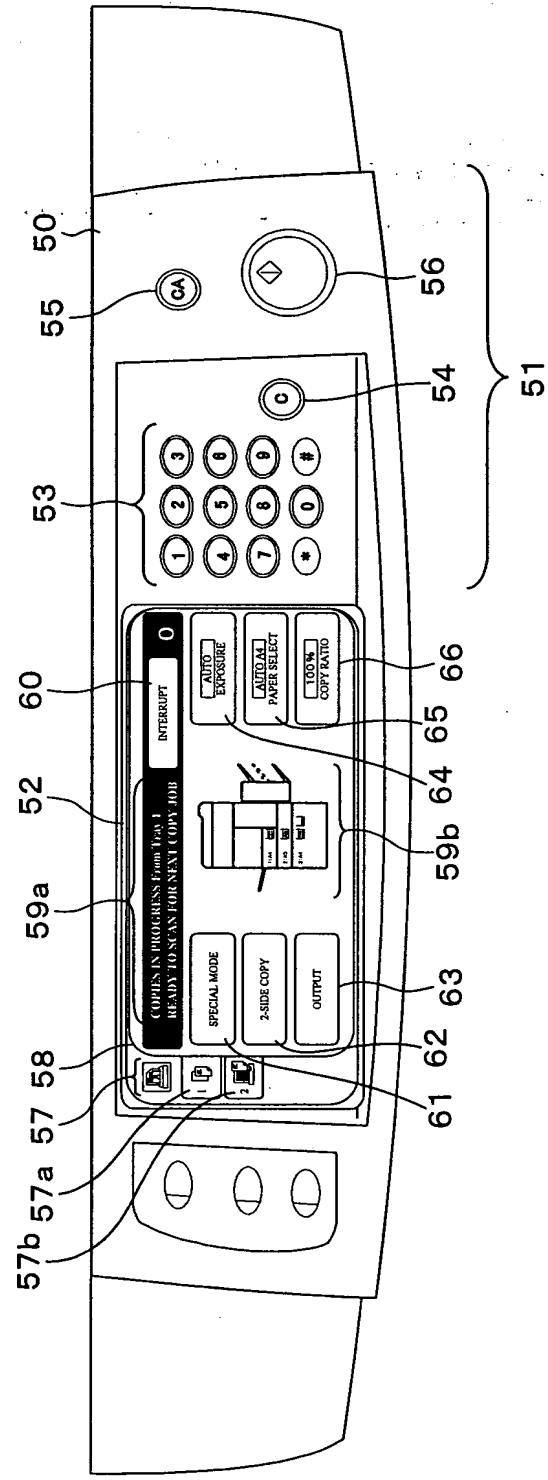


FIG. 5

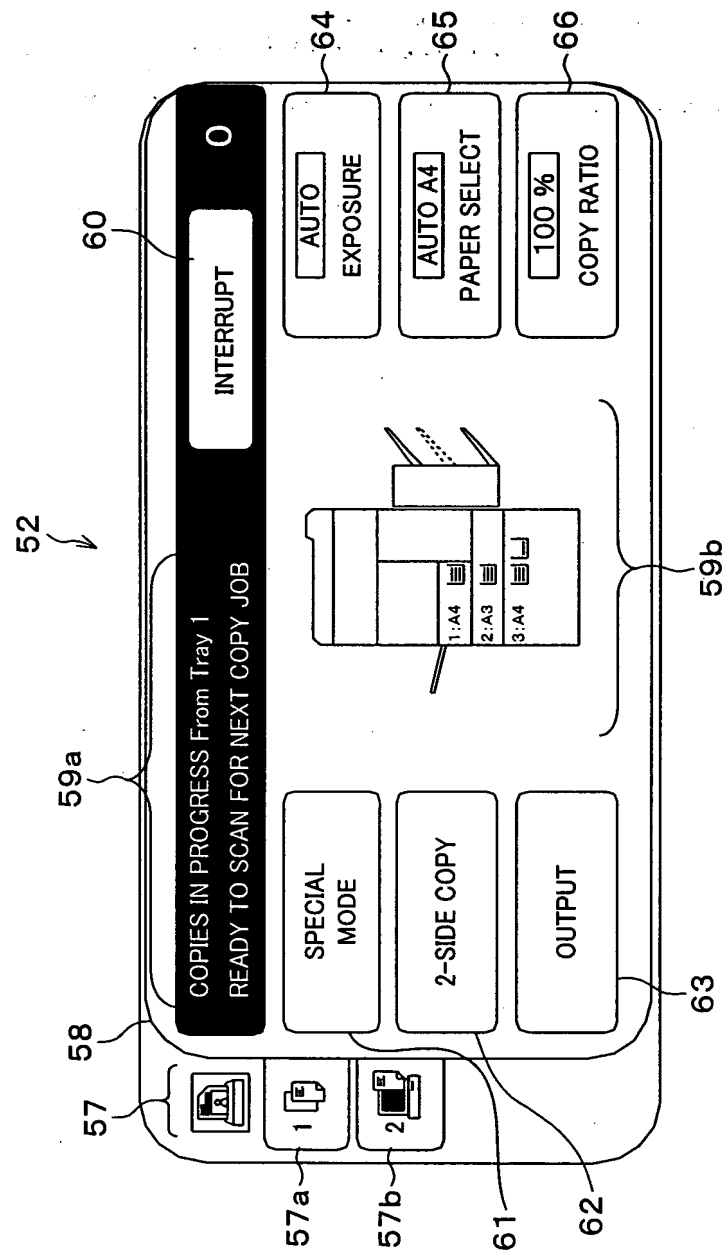


FIG. 6

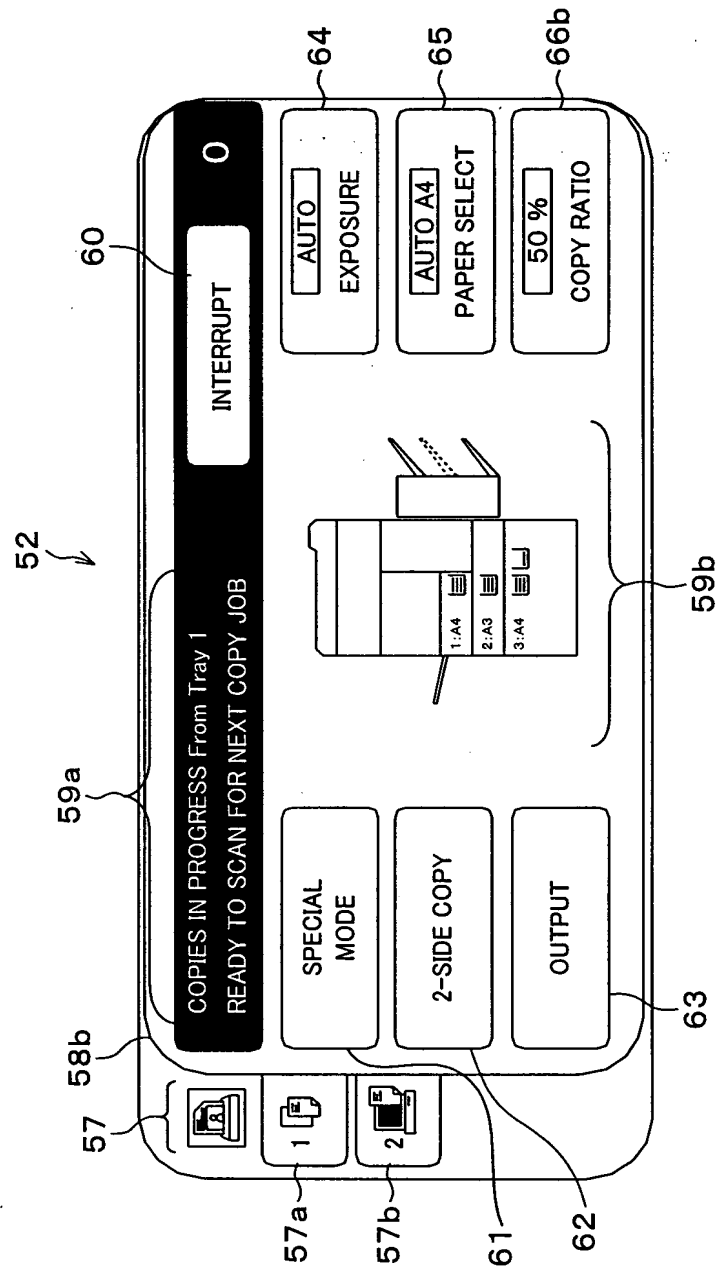


FIG. 7

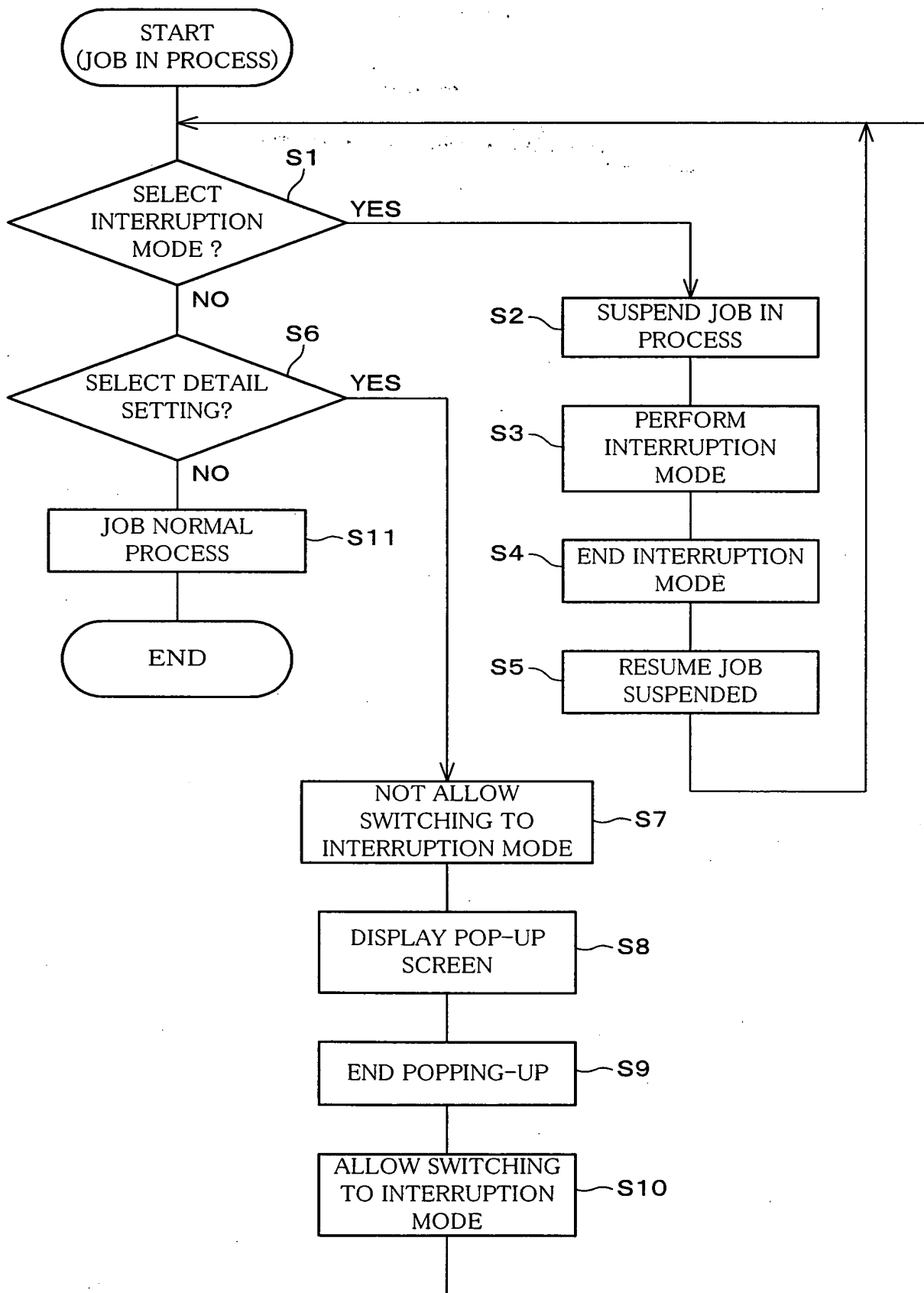


FIG. 8

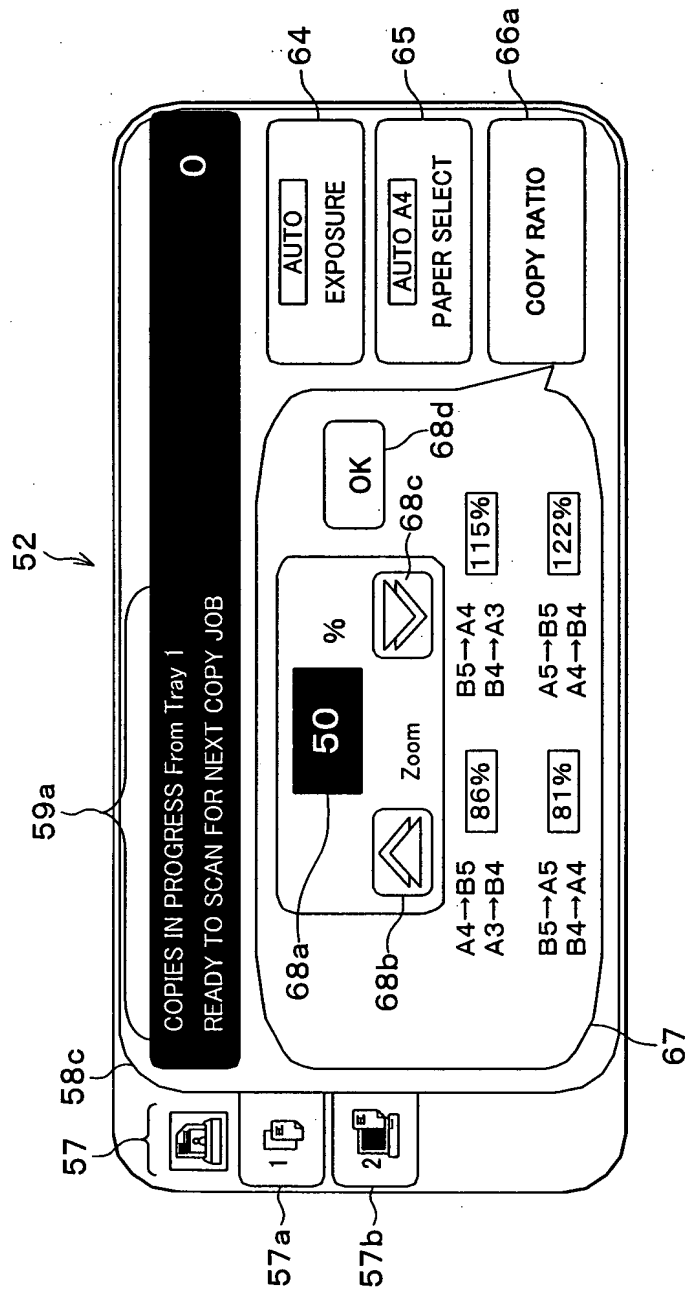




FIG. 9

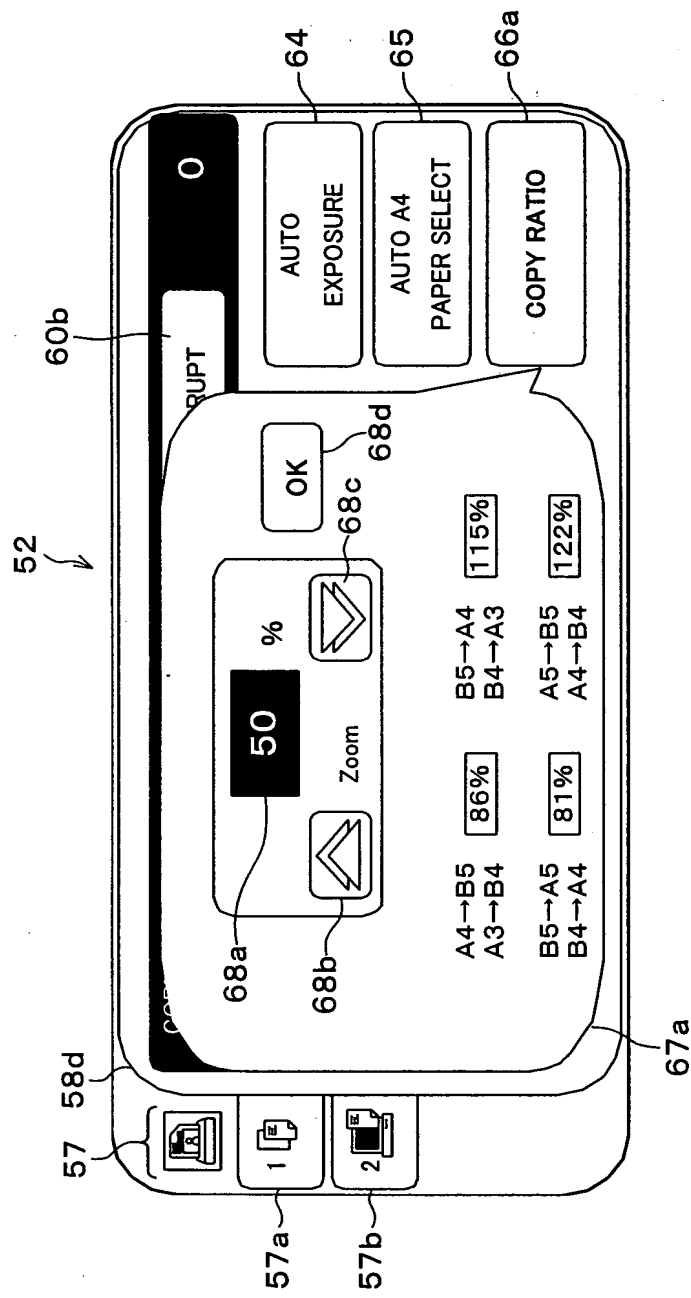


FIG. 10

